

MS-6714

Version : 2.0A

INTEL (R) Brookdale-G GE/PE Chipset

Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU: Willamette/Northwood mPGA-478B Processor

System Brookdale-G / GE / PE Chipset:

INTEL GMCH + ICH4

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF-AW

Clock Generator -- CY28349

AC'97 Codec -- RealTek AC650

Onboard Lan Chipset-- RealTek RTL8101L


Expansion Slots:

AGP2.0 SLOT * 1

PCI2.2 SLOT * 3

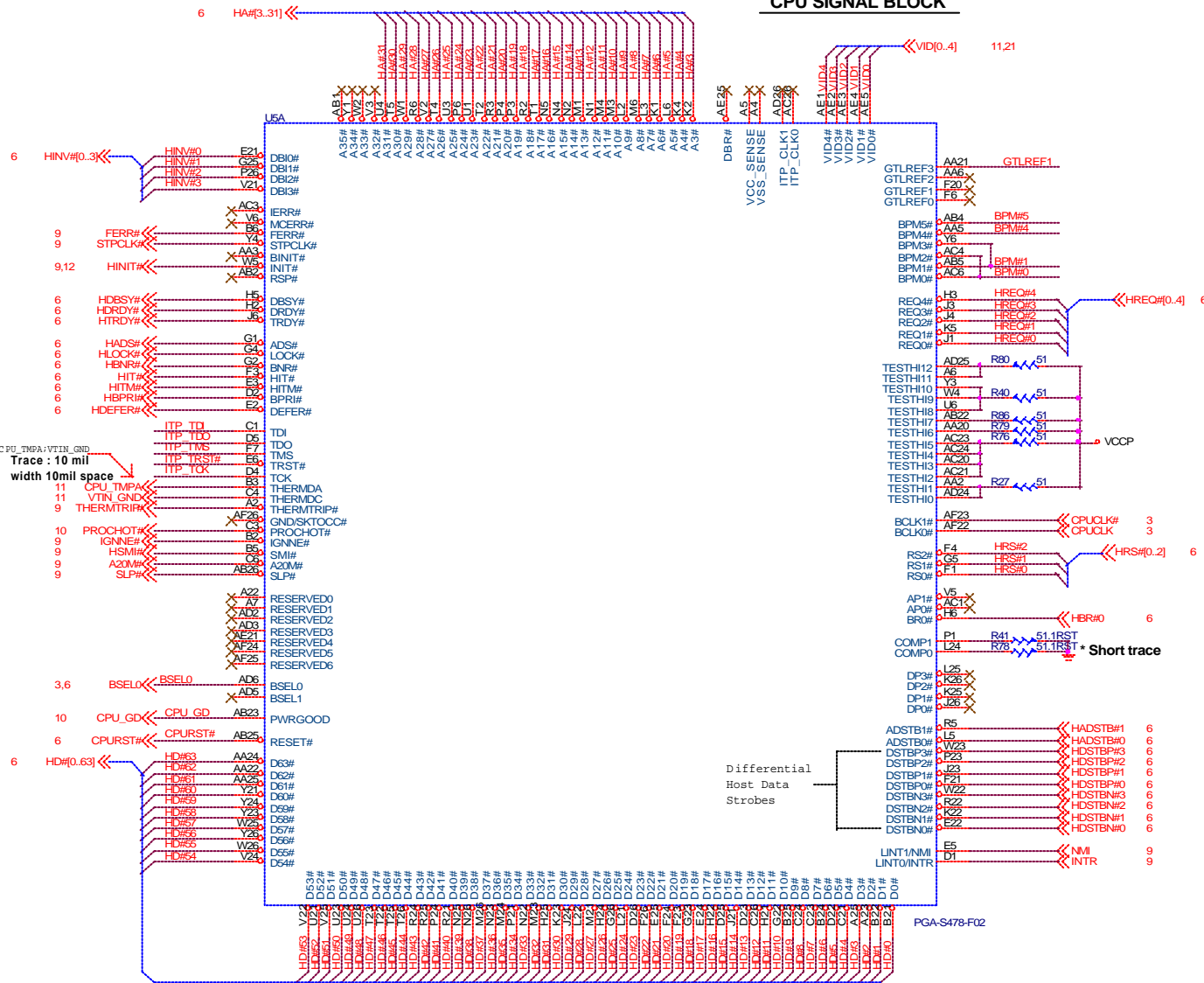
Platform: Micro ATX

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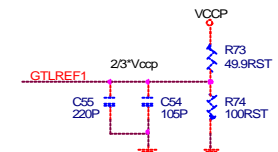
		MICRO-STAR	
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CPU SIGNAL BLOCK

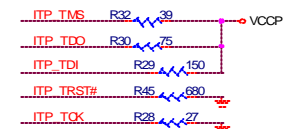


CPU GTL REFERENCE VOLTAGE BLOCK



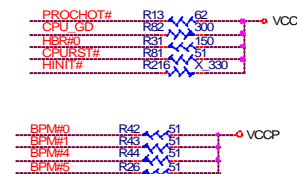
Every pin put one 220pF cap near it.
Trace Width 10mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP BLOCK



ALL COMPONENTS CLOSE TO CPU

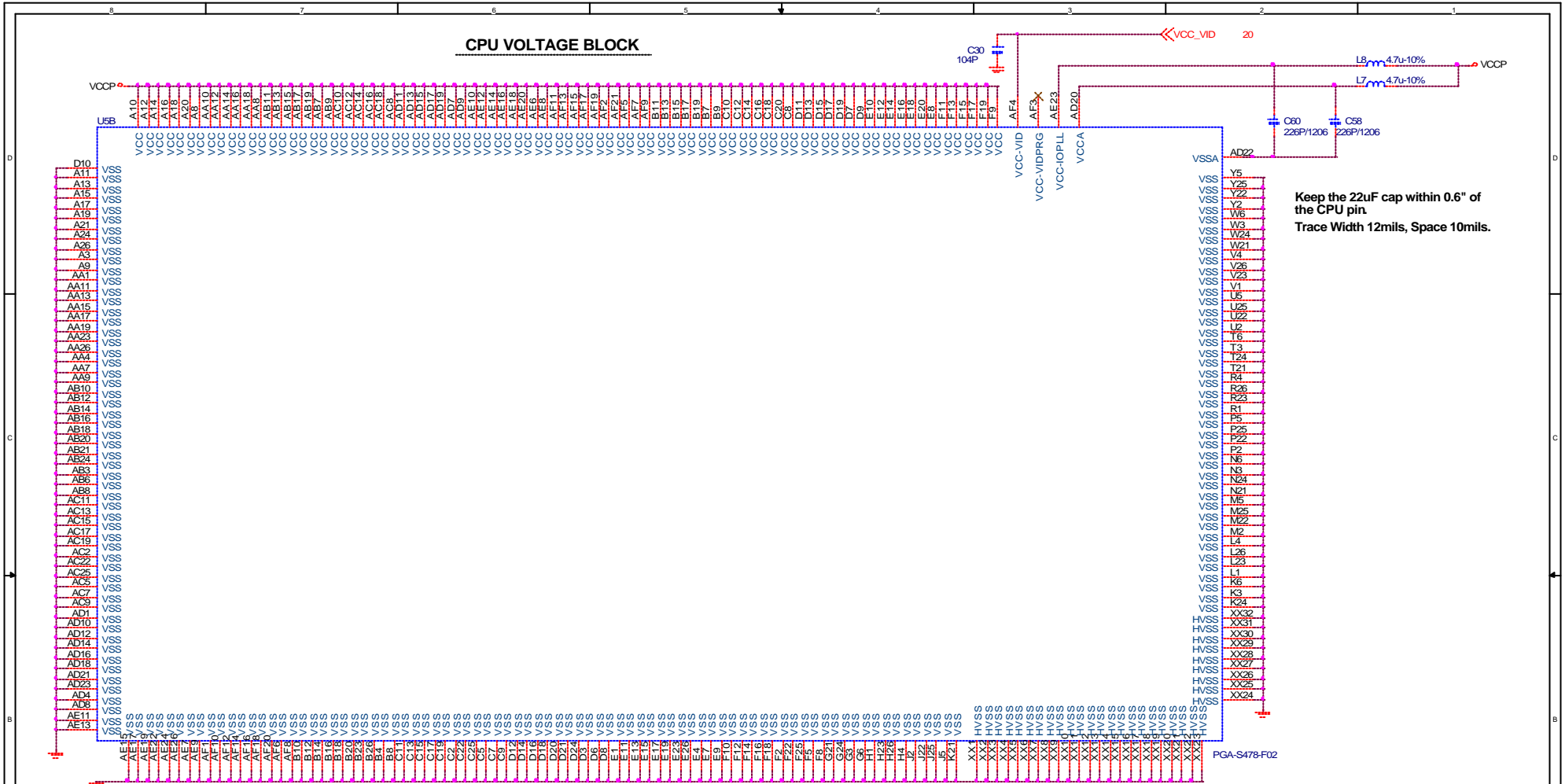
CPU STRAPPING RESISTORS



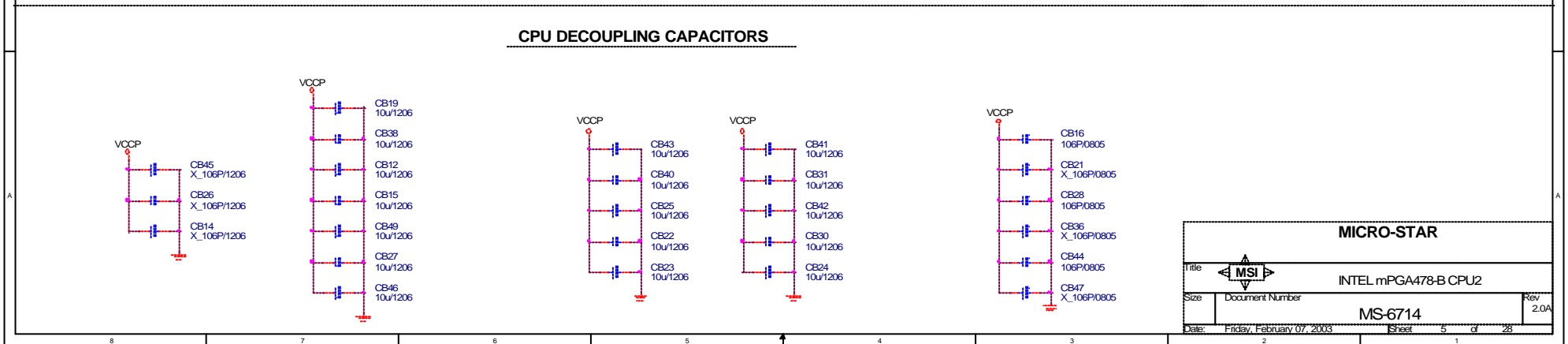
MICRO-STAR

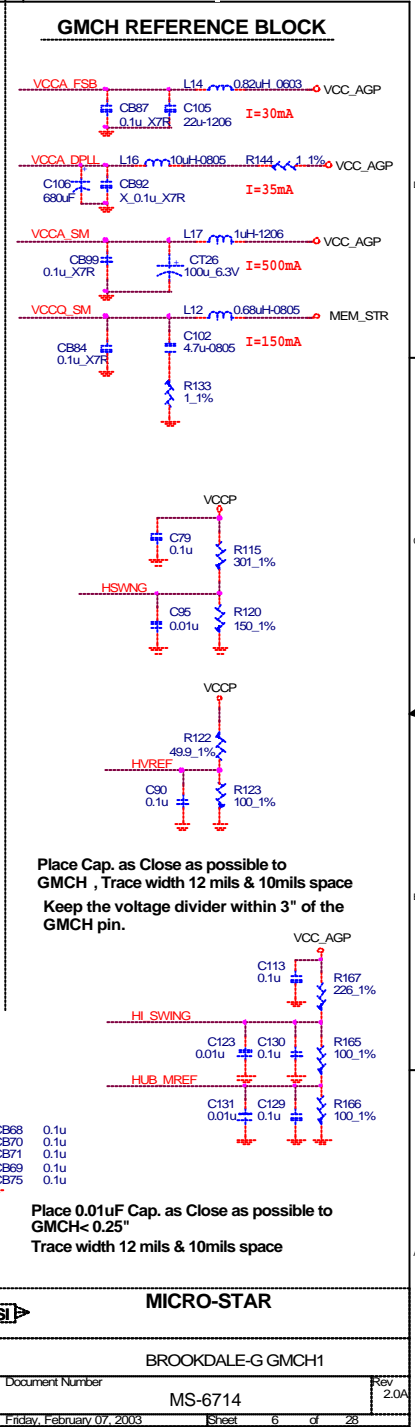
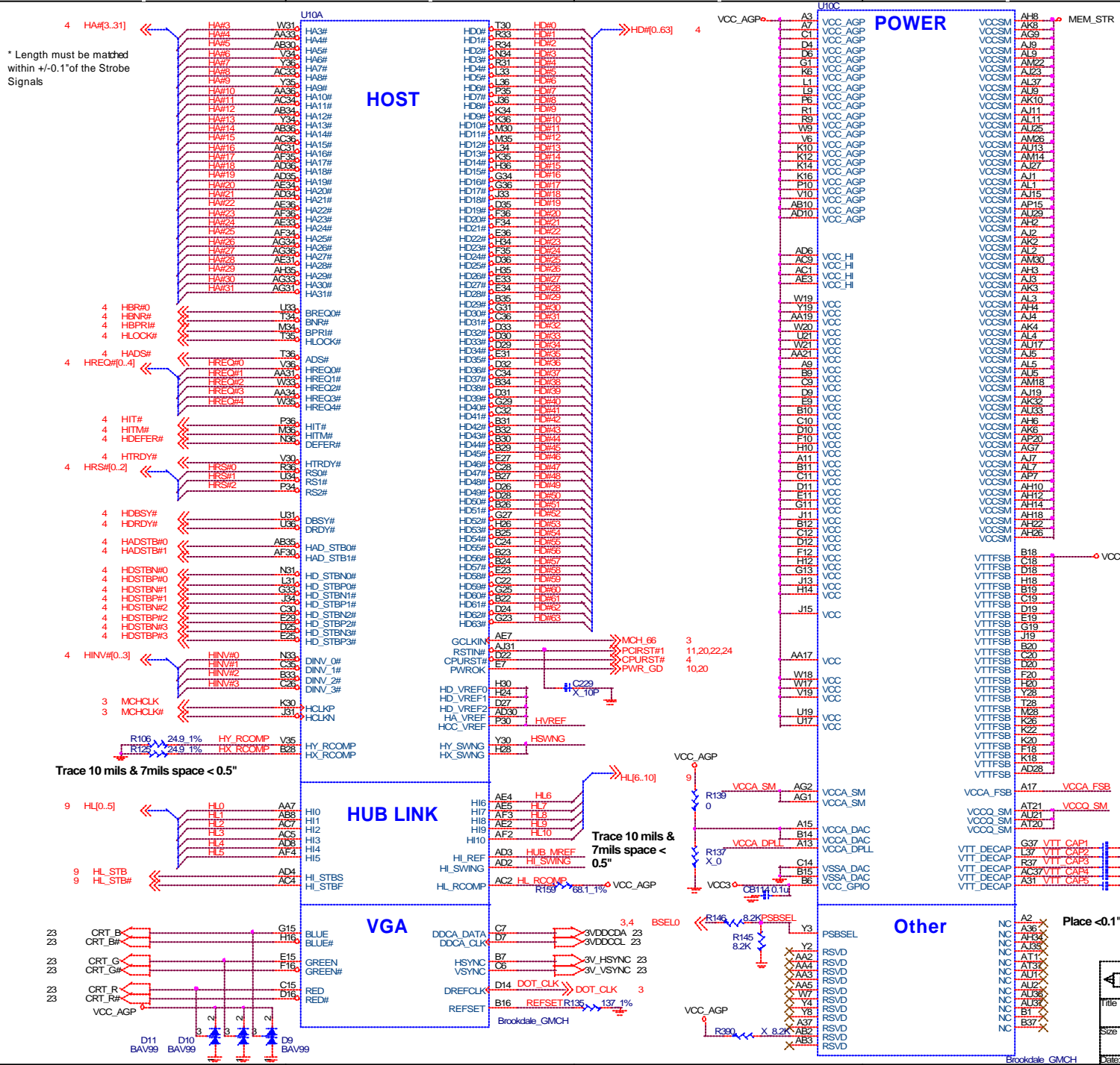
Title				INTEL mPG478 CPU1			
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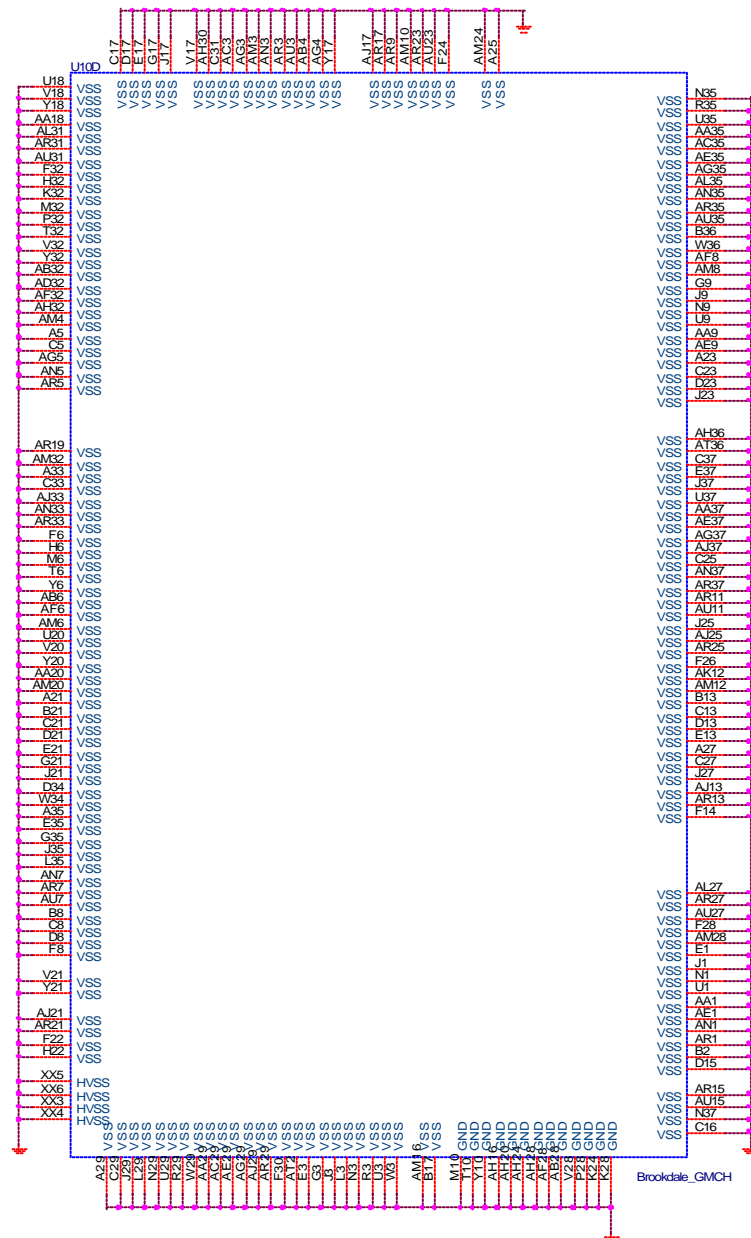
CPU VOLTAGE BLOCK



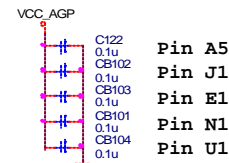
CPU DECOUPLING CAPACITORS







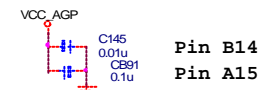
GMCH DECOUPLING CAPACITOR



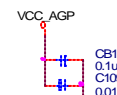
Place decoupling cap
close to GMCH AGP
Interface < 0.1"



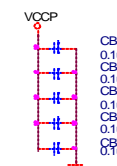
Place decoupling cap
close to GMCH
Hub-Link Interface<
0.1"



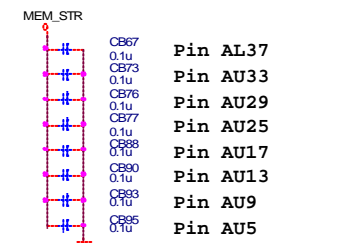
Place decoupling cap
close to GMCH DAC
Interface < 0.1"



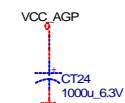
Place decoupling cap
close to GMCH Core
Logic Interface <
0.1"



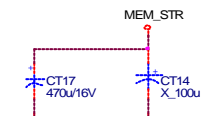
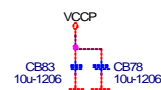
Place decoupling cap
close to GMCH CPU
Interface < 250mil
in the Vtt corridor



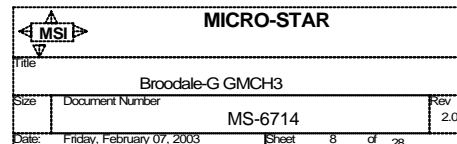
Place decoupling cap
close to GMCH Memory
Interface < 0.1", with
18 mil track width



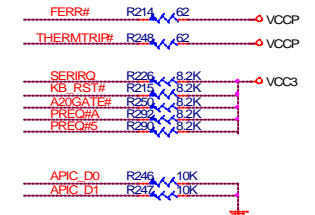
Place Bulk cap for Core Logic,
AGP & Hub Link Interface



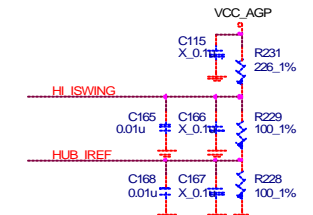
Place Bulk cap between
GMCH & DIMM slot



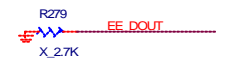
ICH4 PULL-UP/DOWN RESISTORS



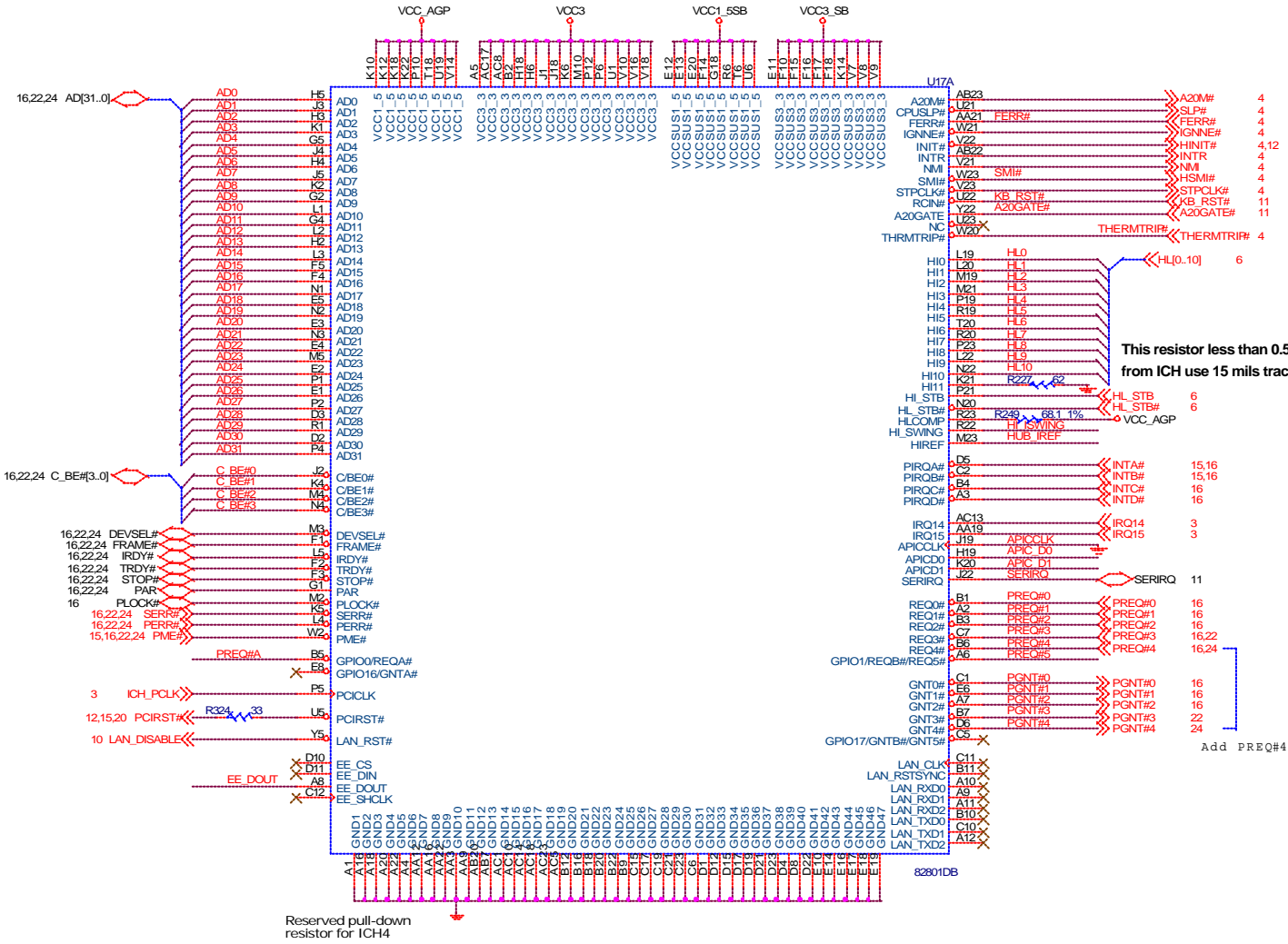
ICH4 REFERENCE VOLTAGE



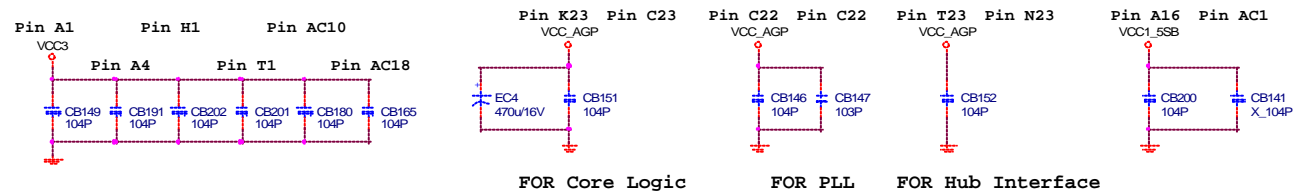
Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space



Add PREQ#4 and GNT#4 to 1394

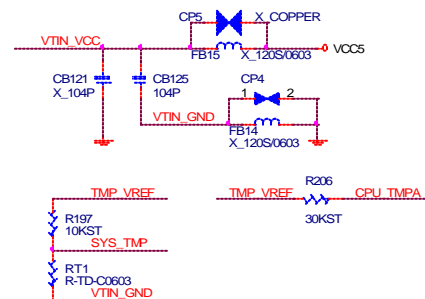
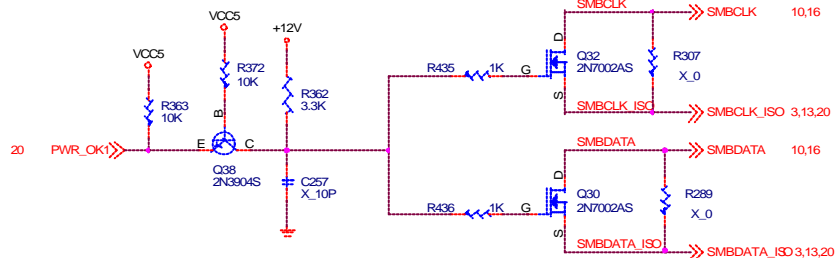
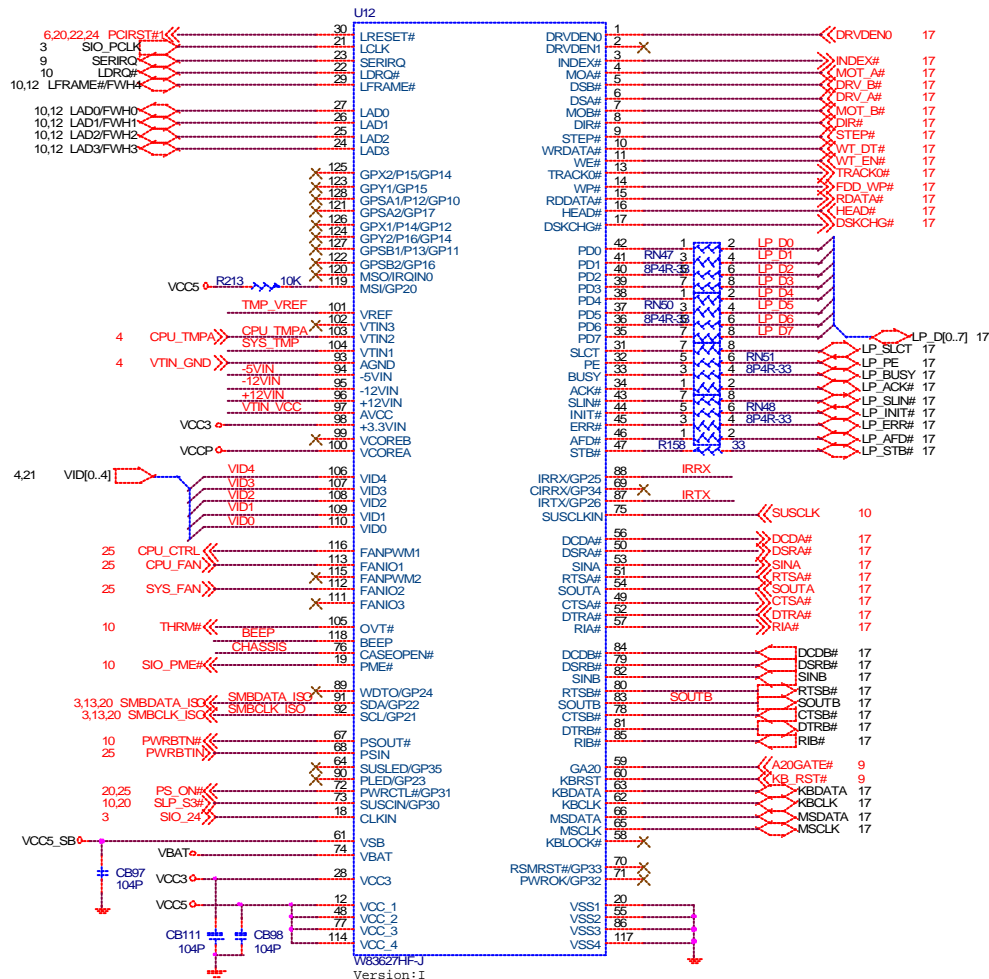


ICH4 DECOUPLING CAPACITORS Place one 0.1u close to ICH4 <100 mil

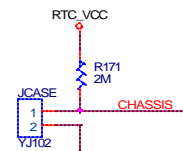


MICRO-STAR

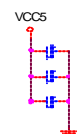
U12



BTC: VCC



VICCE



VOC5 R156 4.7K SOUTA

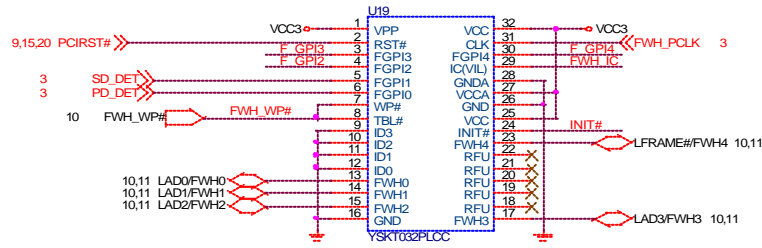


SOUT A	L: Disable KBC	H: Enable KBC
SOUT B	L: 24MHz	H: 48MHz
RTSA#	L: CFAD=2E	H: CFAD=4E
DIRA#	L: PNP Default	H: PNP no Default

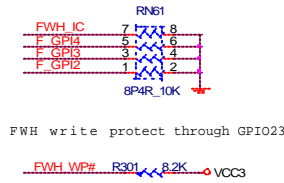


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LPC SUPER I/O			
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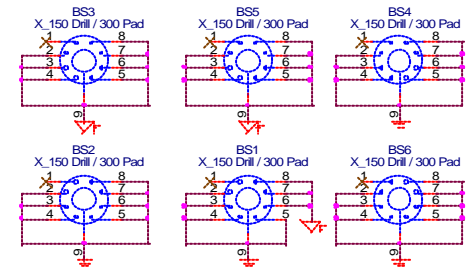
Firware Hub (FWH)



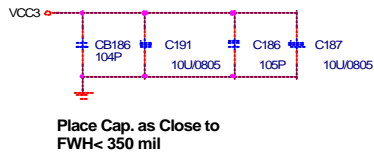
FWH RESISTORS



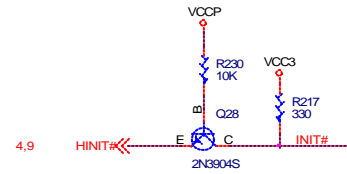
PCB Mounting Holes



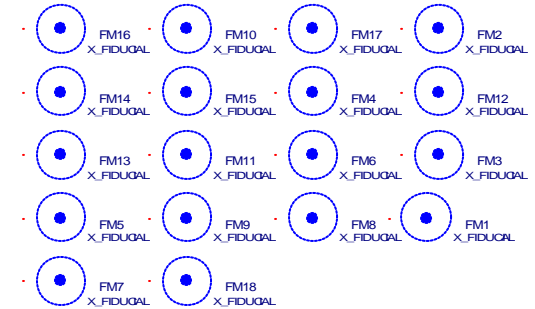
FWH DECOUPLING CAPACITORS



FWH INIT Signal Voltage Translation Block



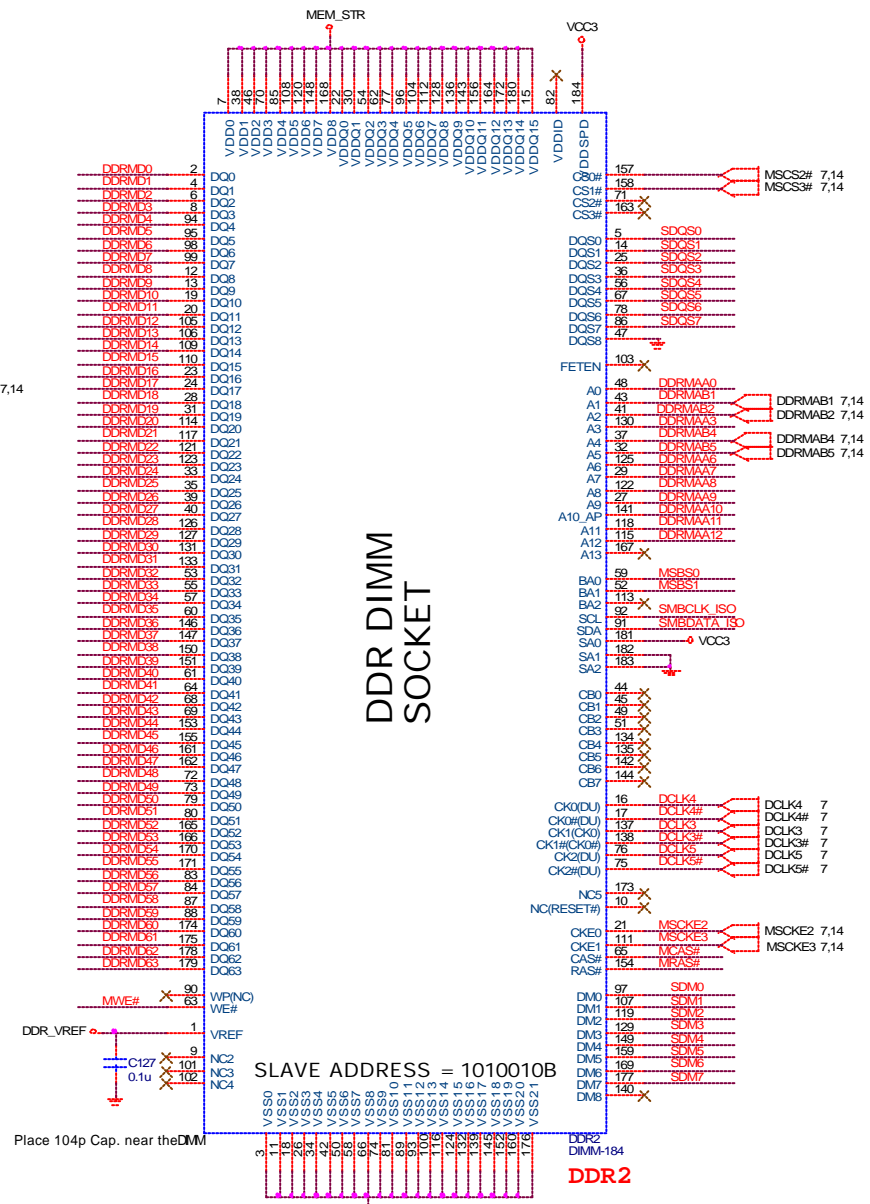
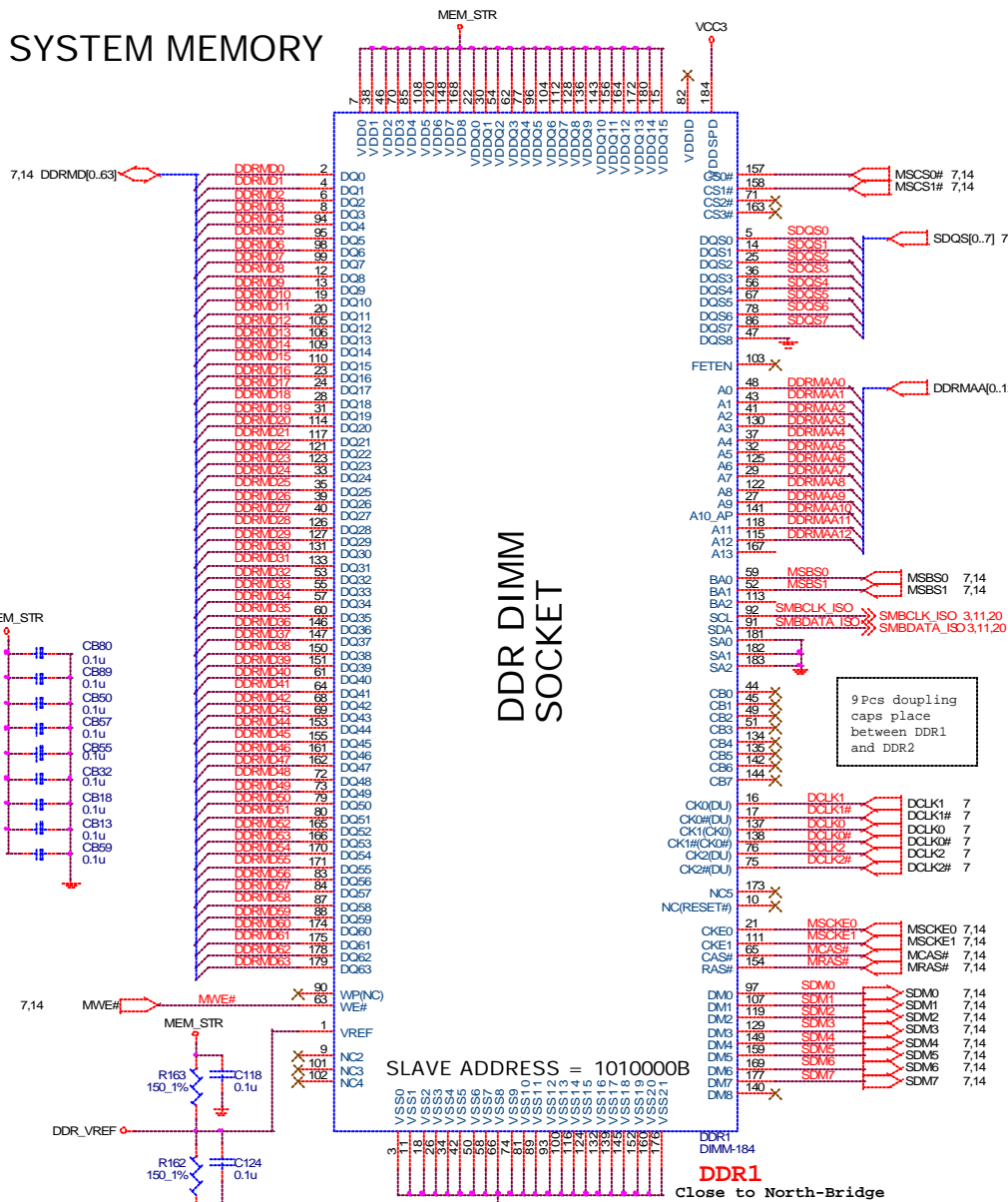
PCB Fiducials



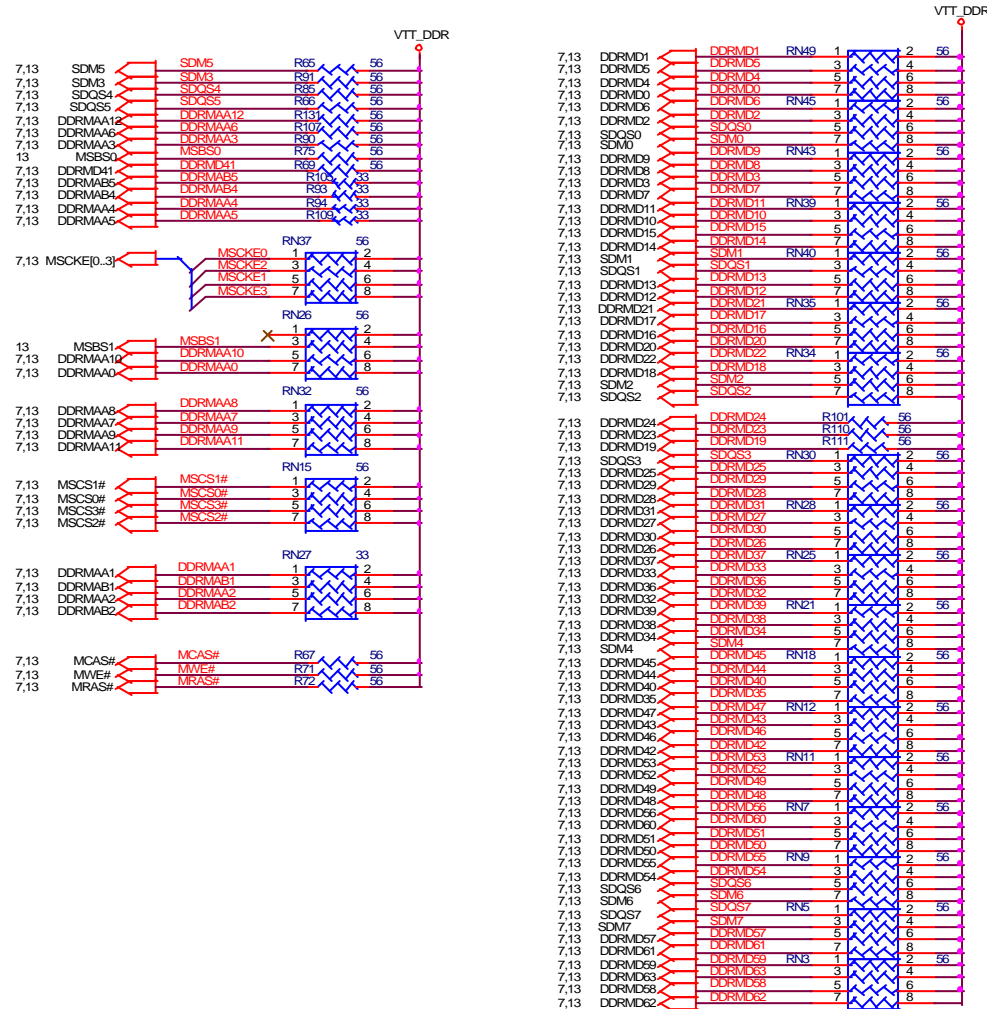
SIMULATION TRACE



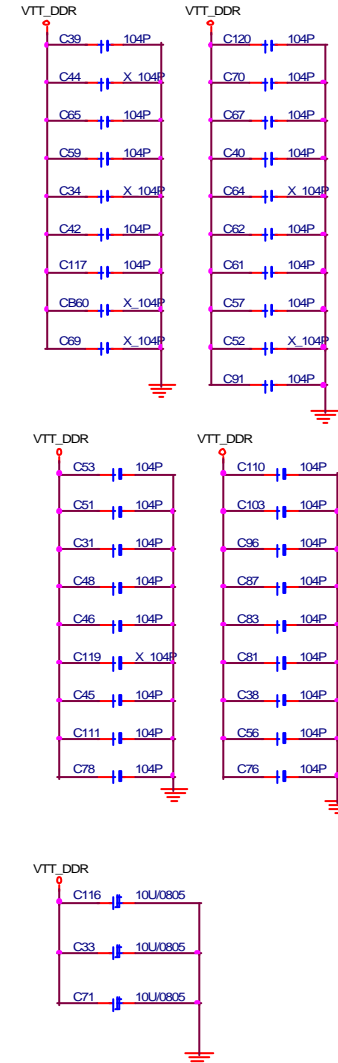
SYSTEM MEMORY



DDR TERMINATORS



TERMINATION DECOUPLING



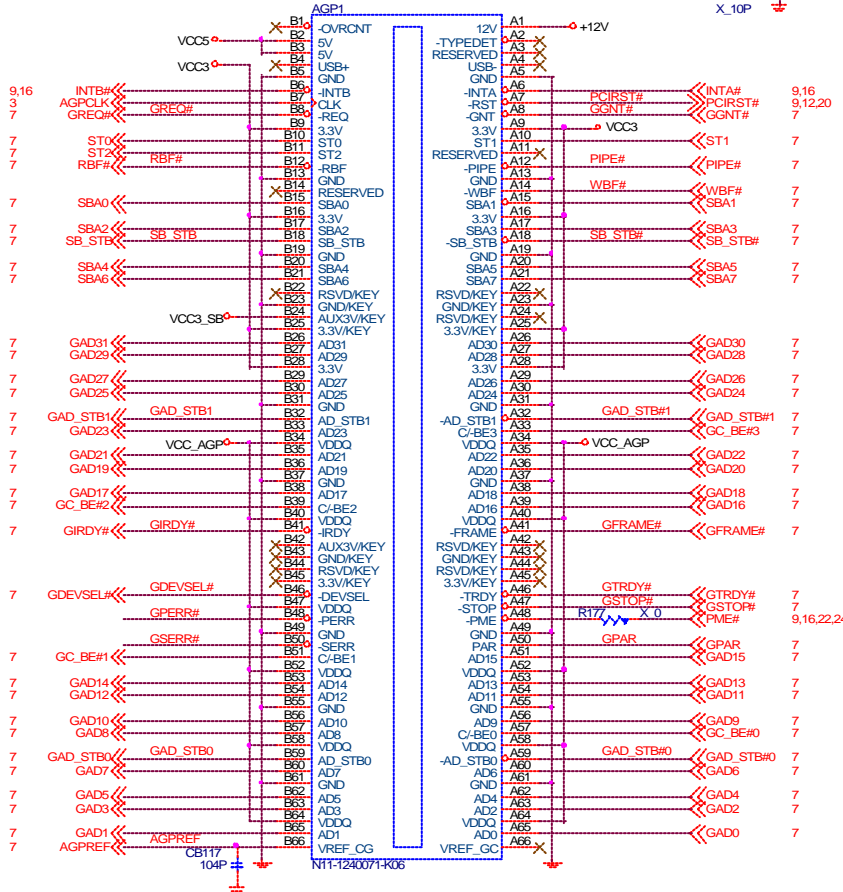
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AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space

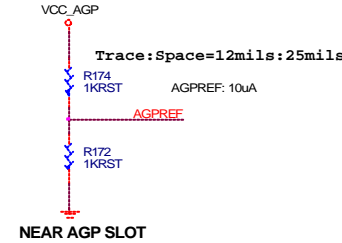
7 ST1[0..2]
7 SBA[0..7]
7 GAD[0..31]
7 GC_BE[0..3]

PCIRST#
X_10P

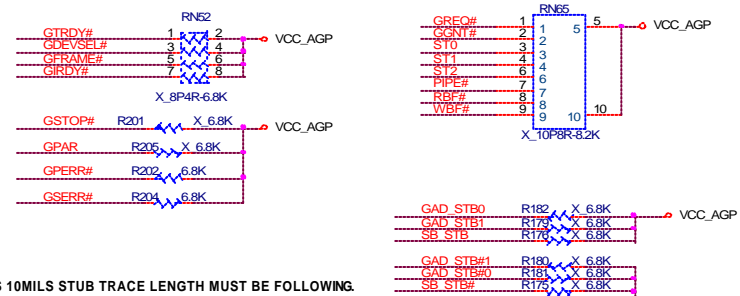


INTA#
INTB#

AGP SIGNAL REFERENCE CIRCUIT

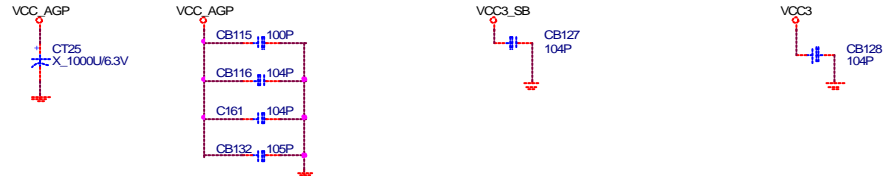


AGP TERMINATION RESISTORS

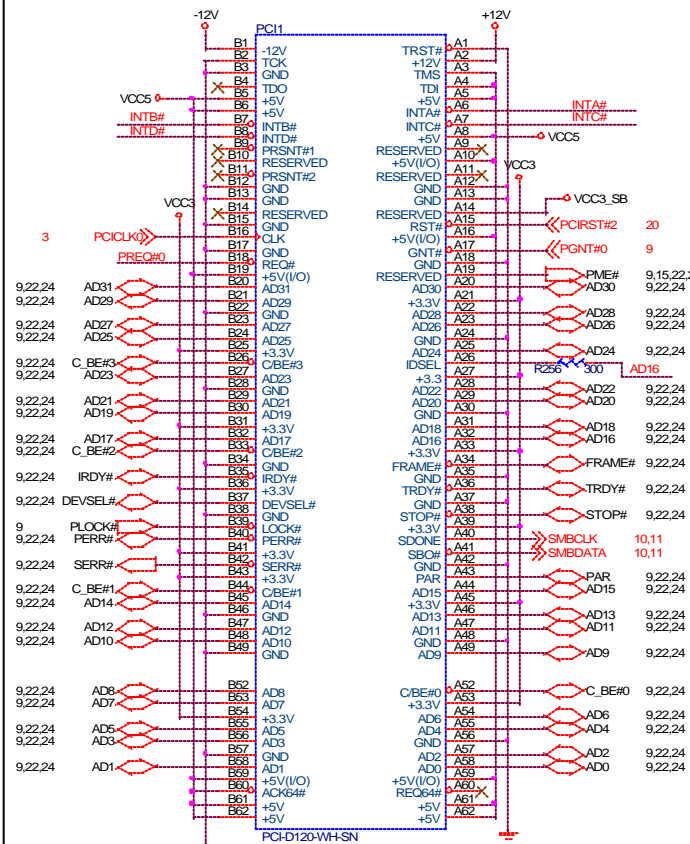


LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING

AGP SLOT DECOUPLING CAPACITORS

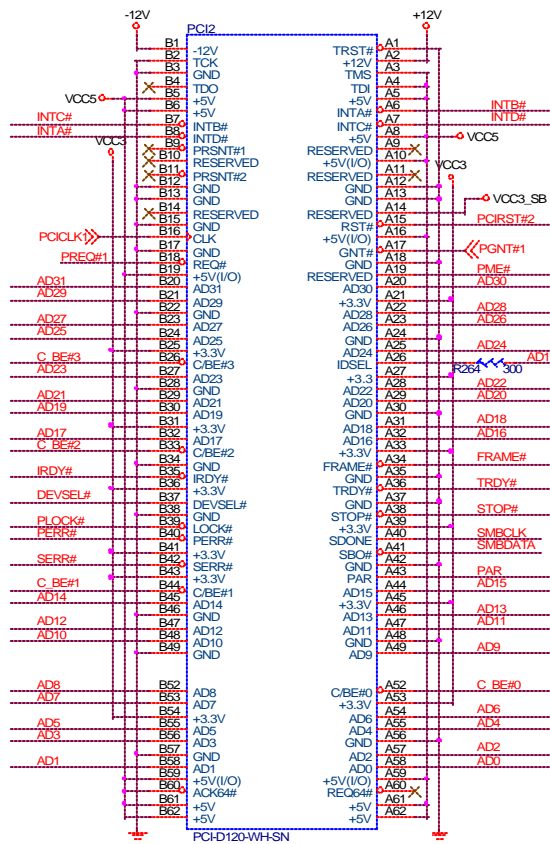


PCI SLOT 1 (PCI VER: 2.2 COMPLY)



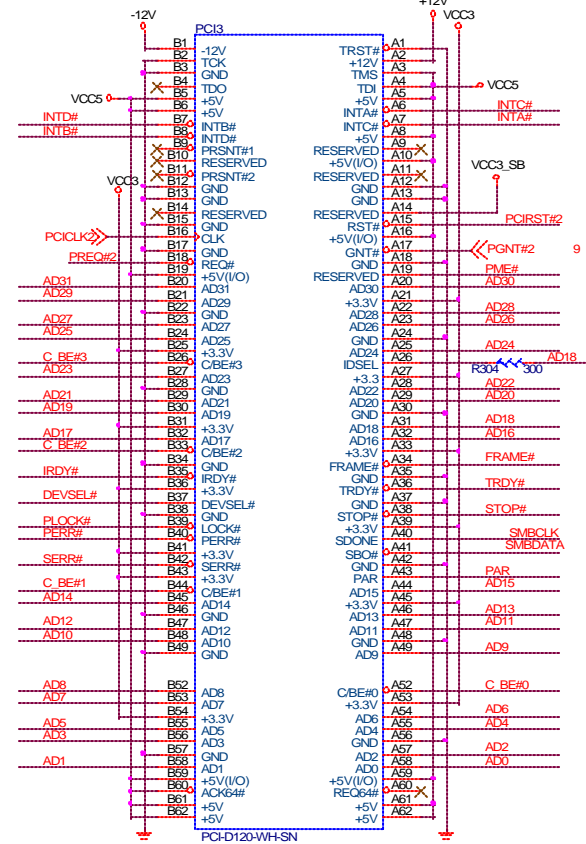
IDSEL = AD16
MASTER = PREQ#0
INT# = ABCD

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



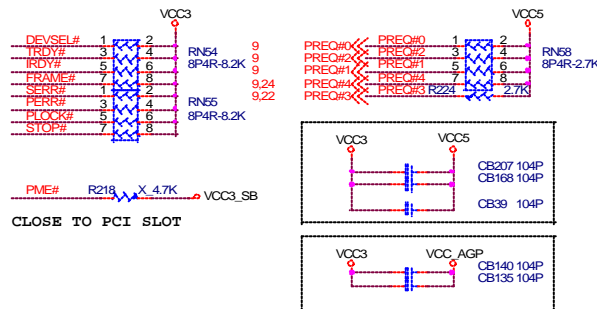
IDSEL = AD17
MASTER = PREQ#1
INT# = BCDA

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

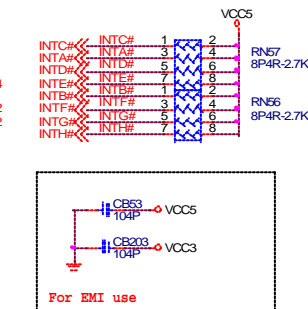


IDSEL = AD18
MASTER = PREQ#2
INT# = CDBA

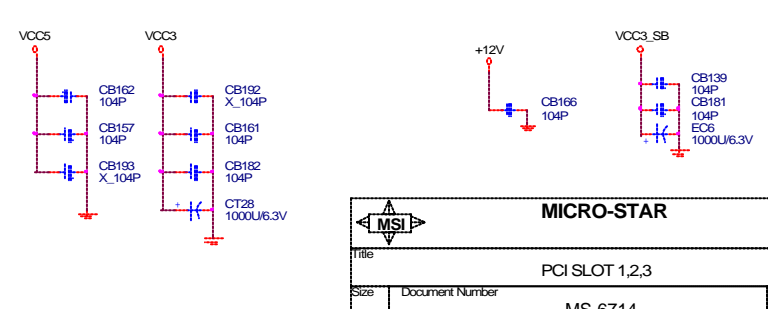
PCI PULL-UP / DOWN RESISTORS



PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



[illegible][illegible]

PS2 KEYBOARD & MOUSE CONNECTOR

FLOPPY CONNECTOR

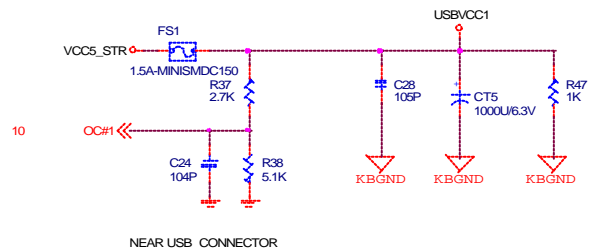
FDD1

Pin	Signal	Direction	
1	2	DRVDEN0	11
5	4		
7	6		
9	8	INDEX#	11
11	10	MOT_A#	11
13	12	DRV_B#	11
15	14	DRV_A#	11
17	16	MOT_B#	11
19	18	DIR#	11
21	20	STEP#	11
23	22	WT_DT#	11
25	24	WT_EN#	11
27	26	TRACK0#	11
29	28	FDD_WP#	11
31	30	RDATA#	11
33	32	HEAD#	11
	34	DSKCHG#	11

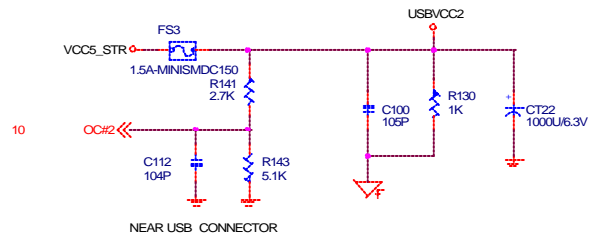
D2x17-1:31-BK



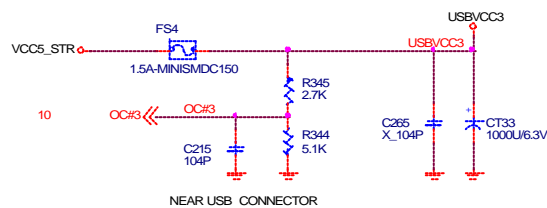
POWER CIRCUIT FOR USB PORT 0,1



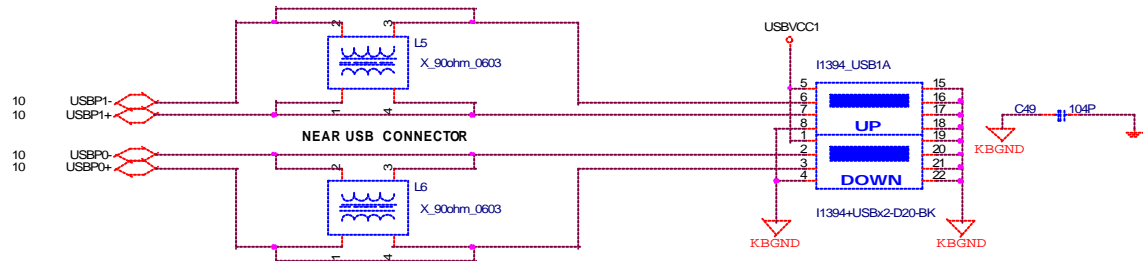
POWER CIRCUIT FOR USB PORT 2,3



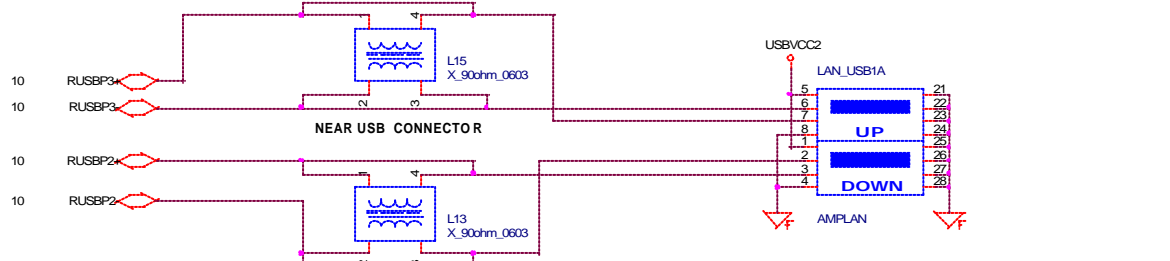
POWER CIRCUIT FOR USB PORT 4,5



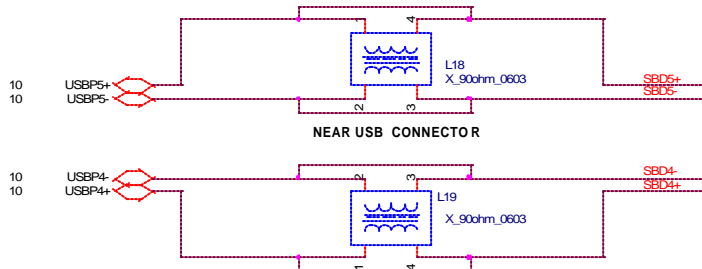
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



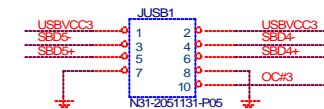
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3 (Shard with Front USB JUSB2)



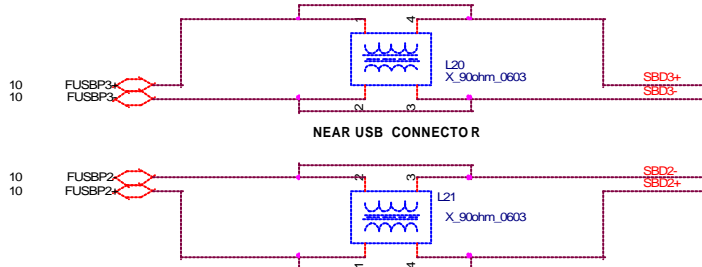
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



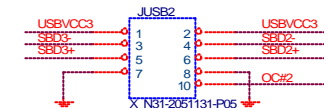
Intel Front USB Header



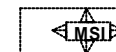
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3 (Shard with rear USB LAN_USB1)



Intel Front USB Header



- * USB Trace width : 7.5 mils
- * USB Trace Spacing : 20 mils
- * Differential USB Signlas Trace, Spacing : 7.5 mils
- * USB Power Trace must be 50mils width



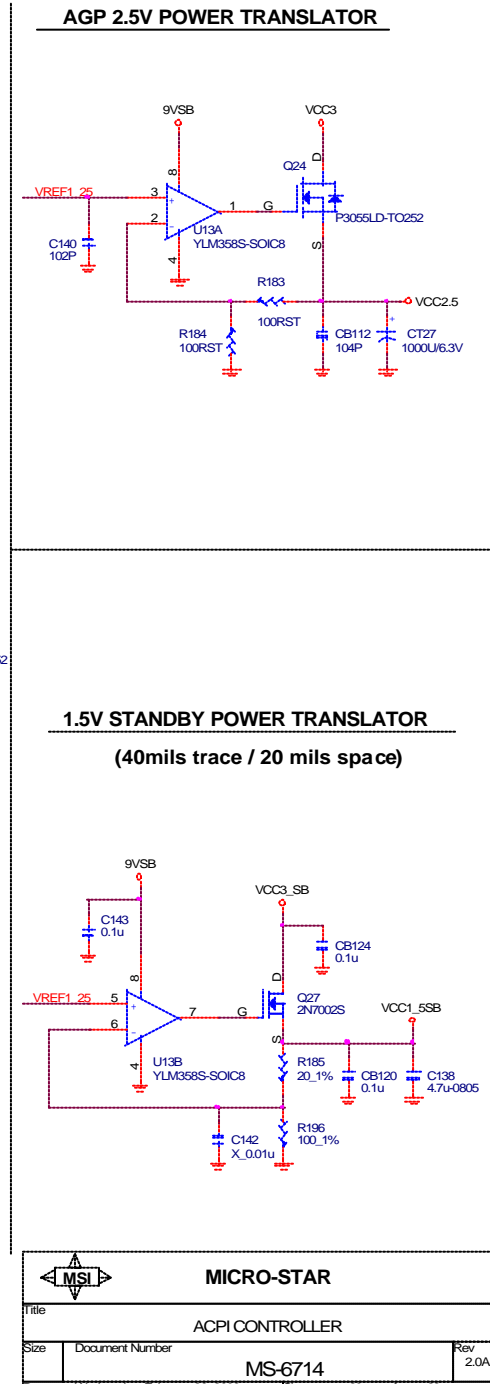
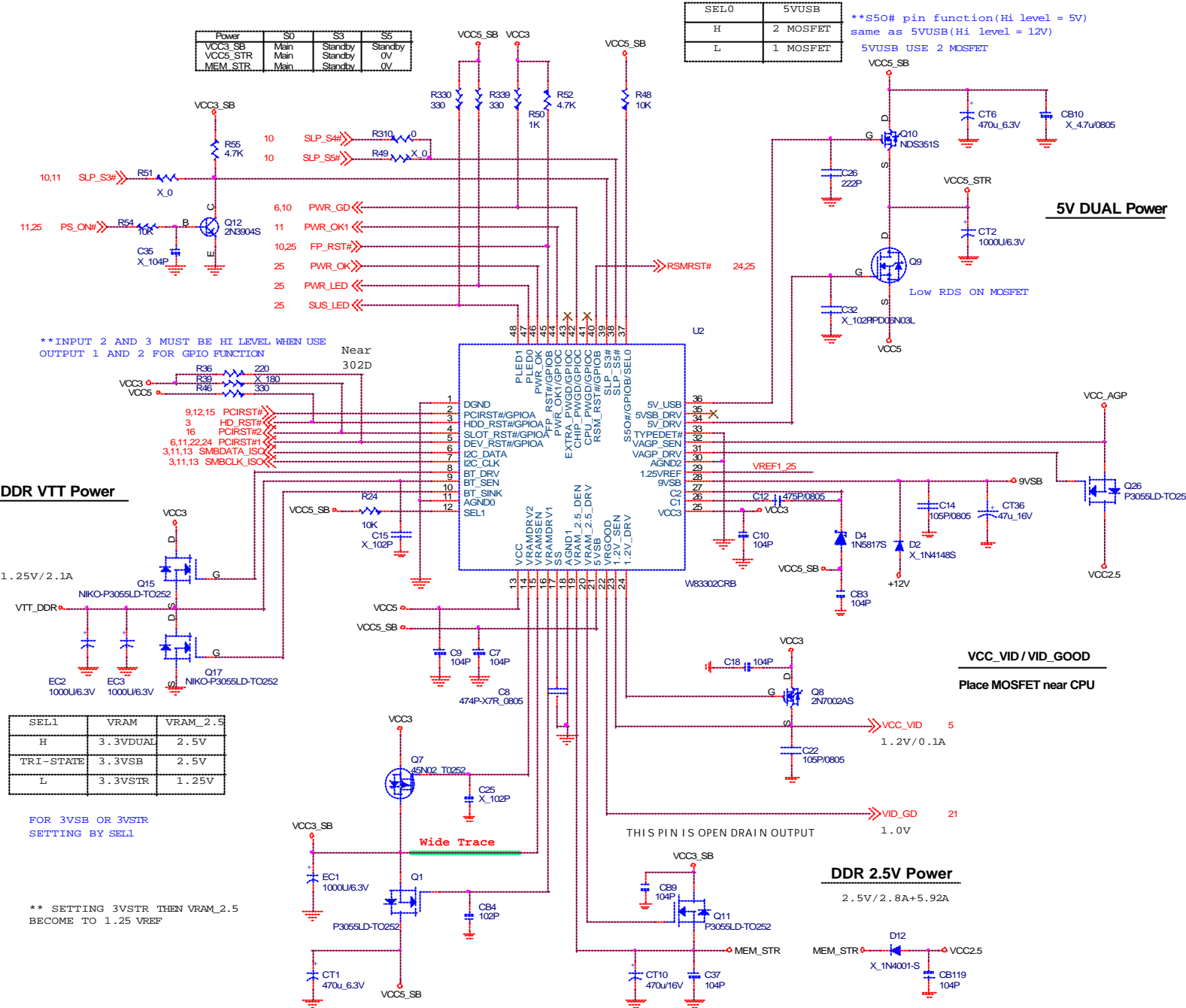
MICRO-STAR

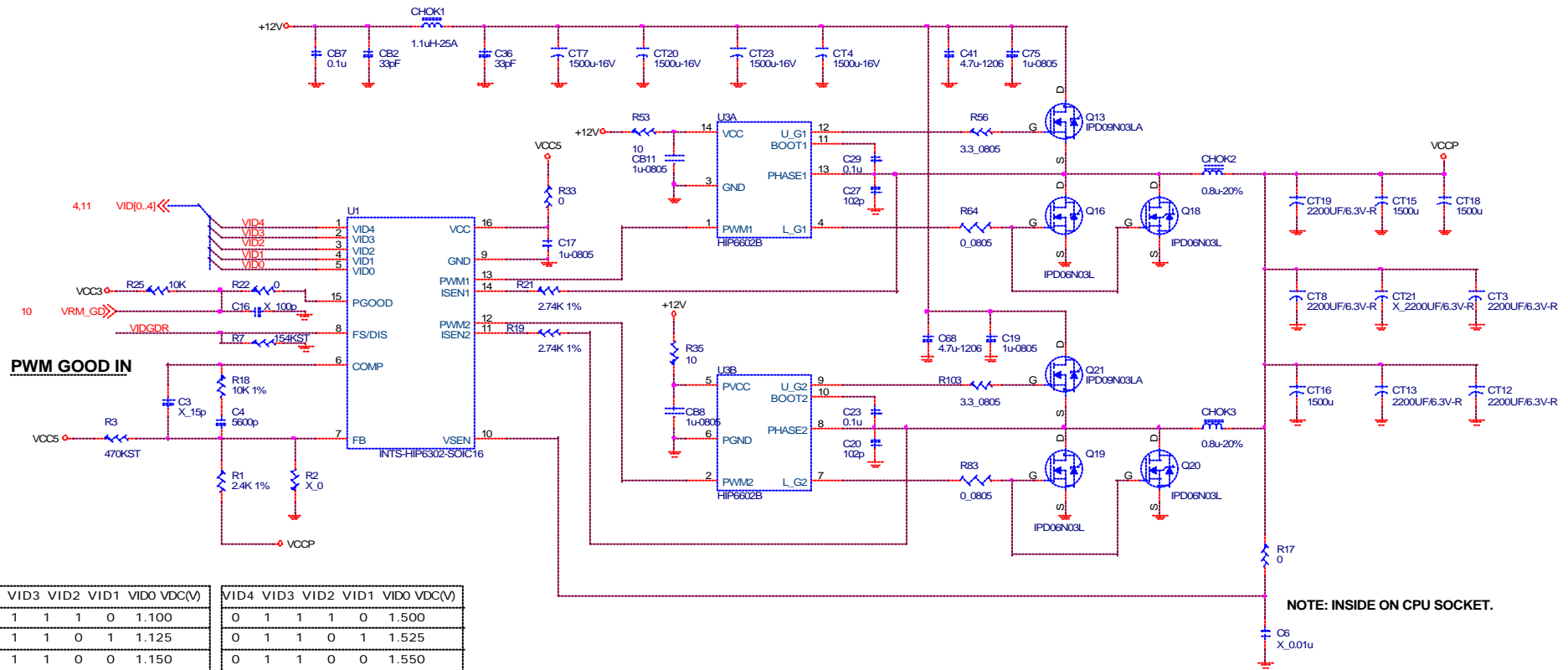
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USB CONNECTORS			
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Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

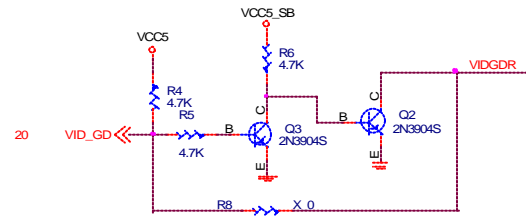
**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET



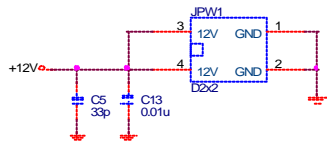


VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

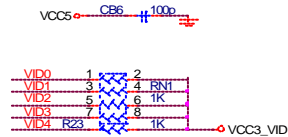
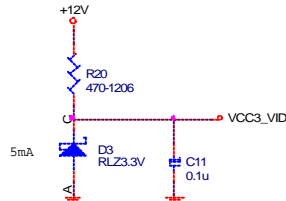
VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF



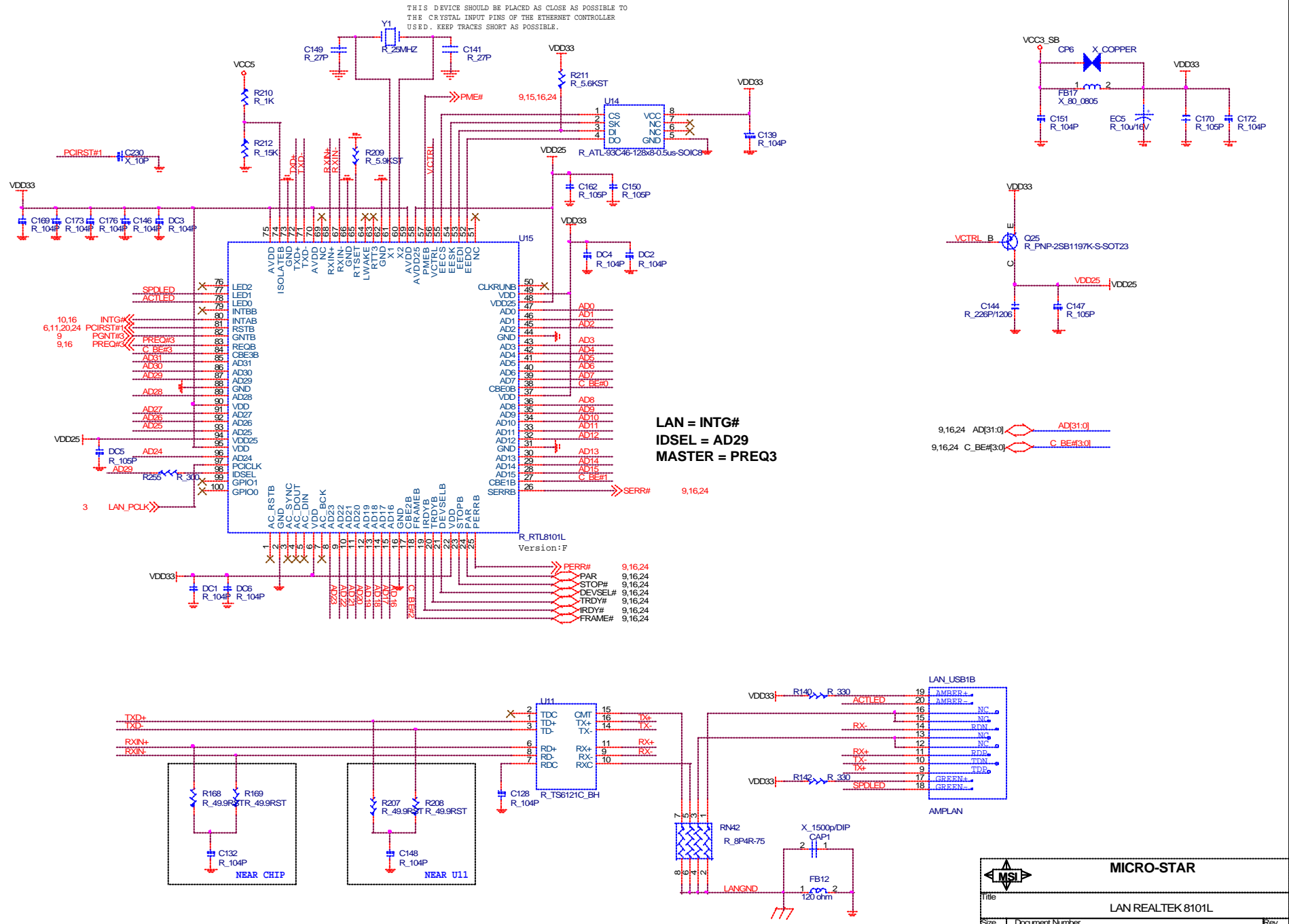
ATX12V POWER CONNECTOR



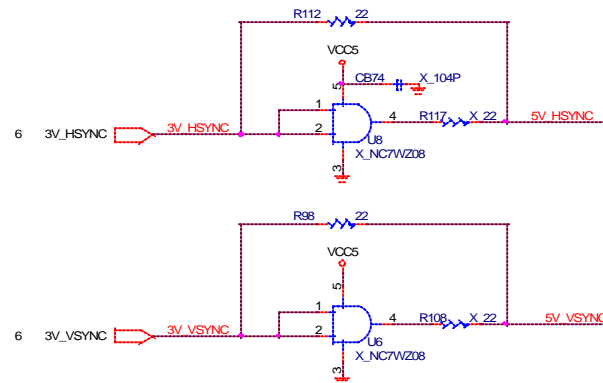
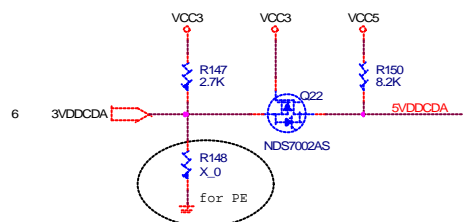
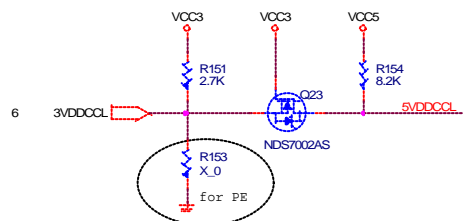
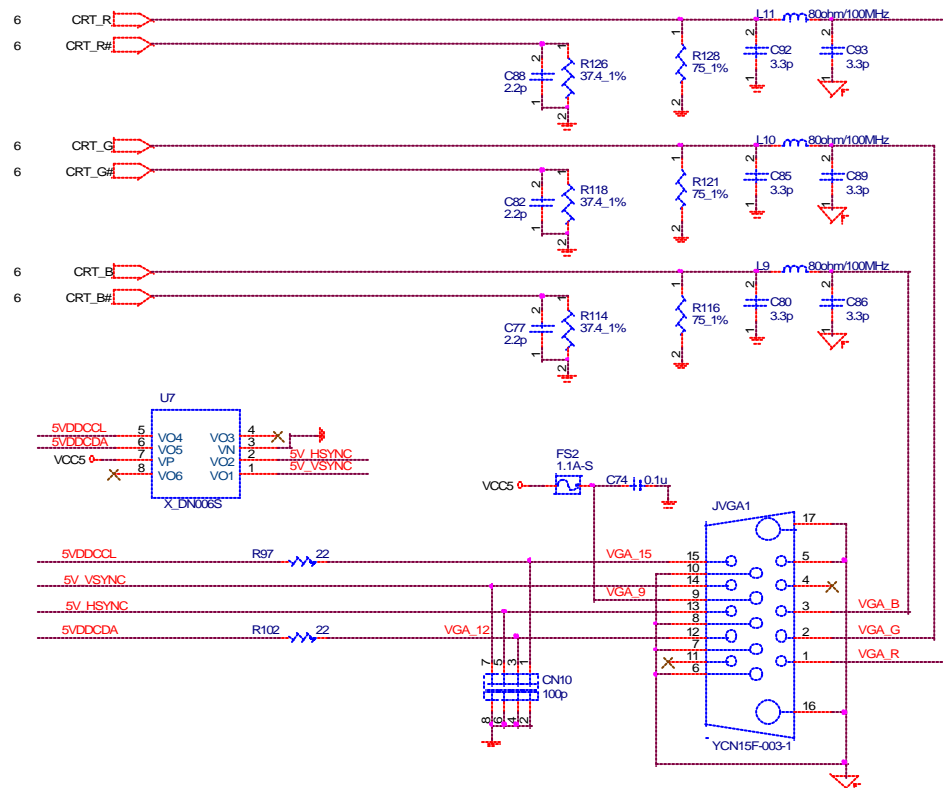
VID PULL-UP RESISTORS

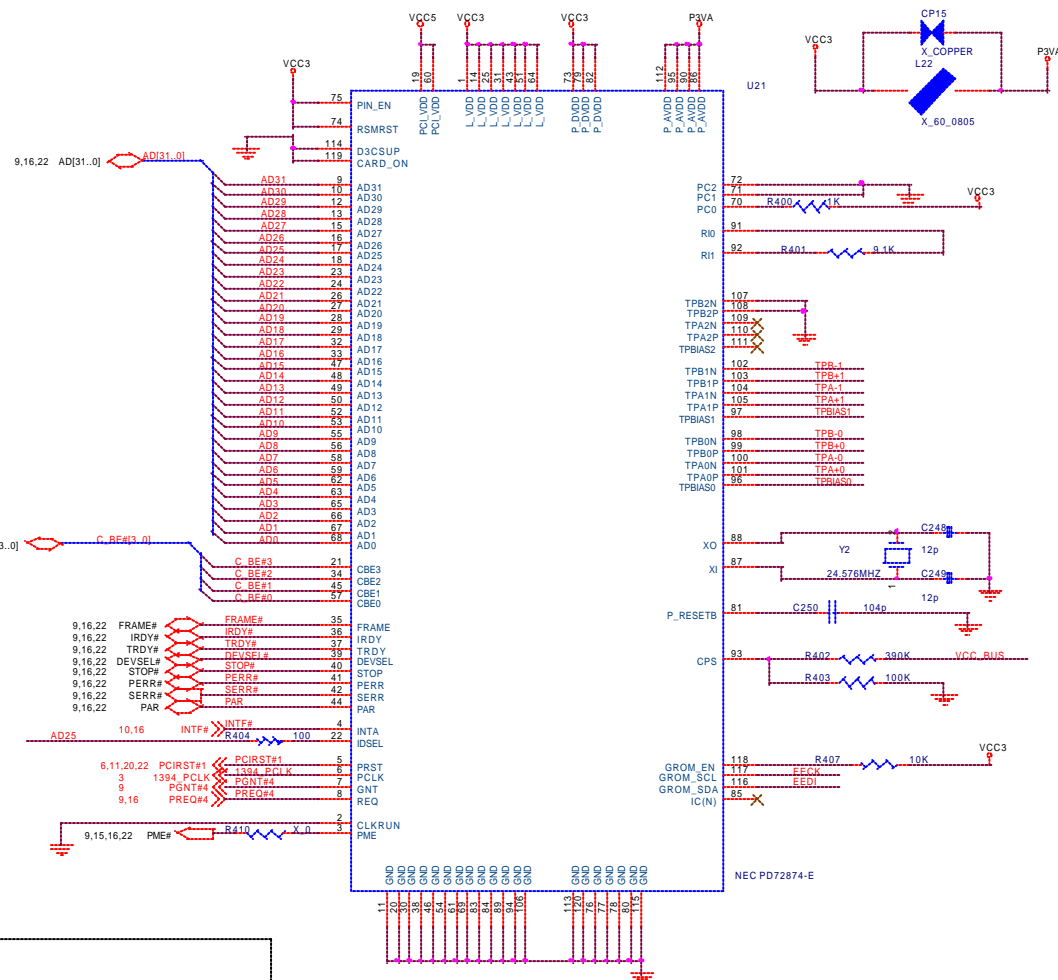
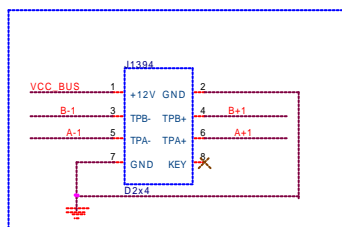
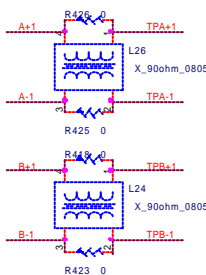
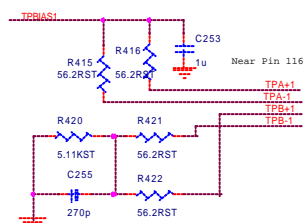
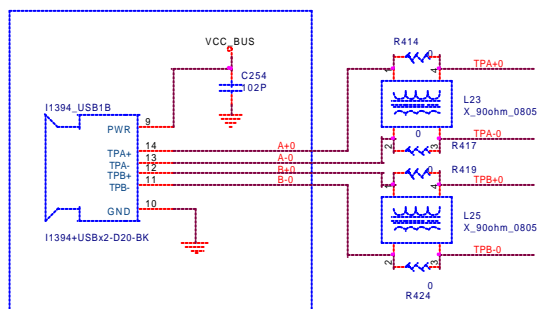
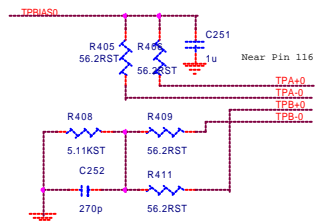


THIS DEVICE SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CRYSTAL INPUT PINS OF THE ETHERNET CONTROLLER USED. KEEP TRACES SHORT AS POSSIBLE.

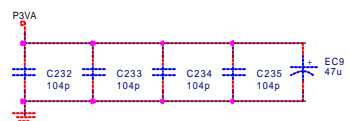


Video Connector

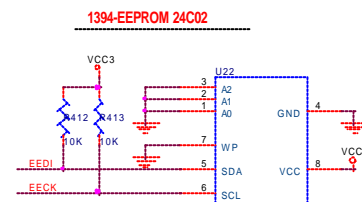
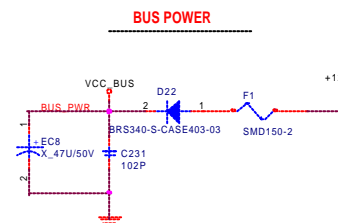
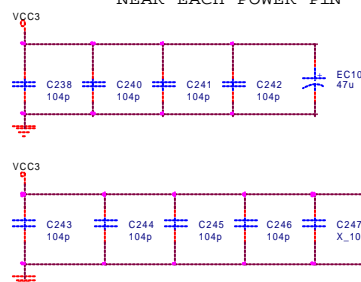




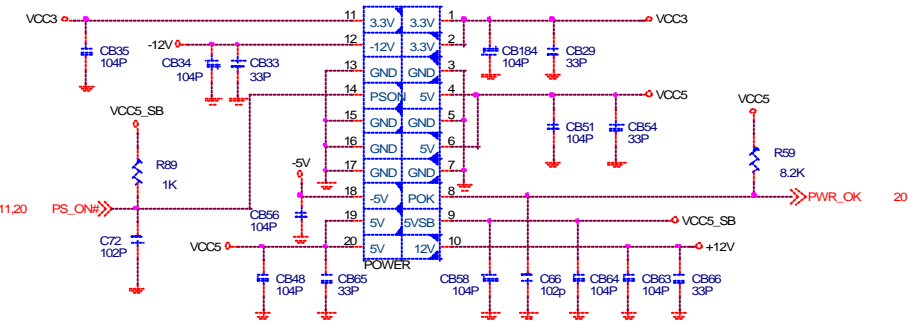
```
IDSEL=AD25
MASTER=PREQ#4
INT#=F
```



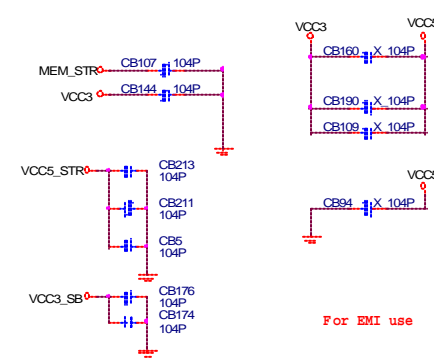
NEAR EACH POWER PIN



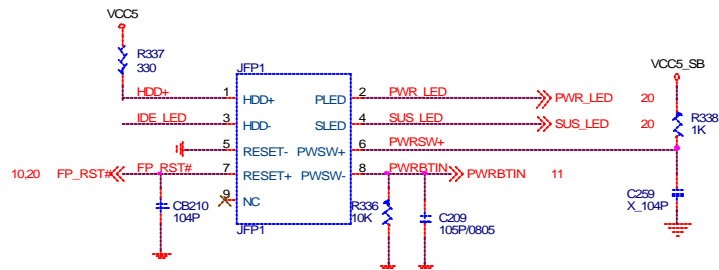
ATX CONNECTOR



REGULATORS OUTPUT DECOUPLING CAPACITORS

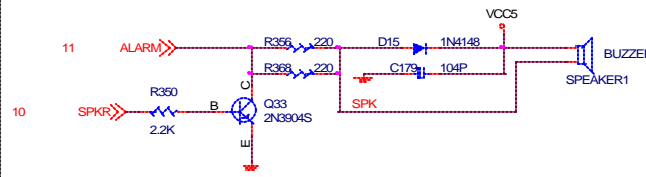


Intel Front Panel

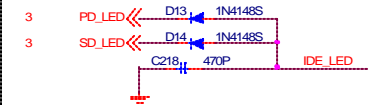


BUZZER

BUZZER always enable

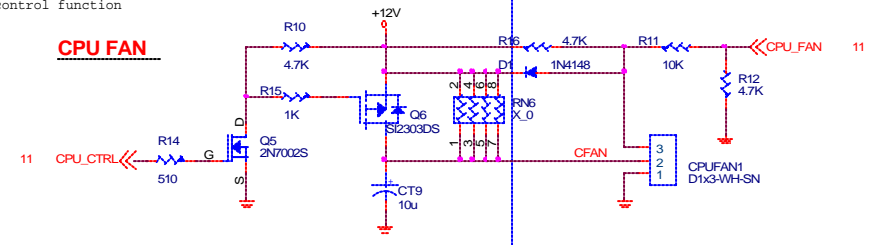


IDE LED

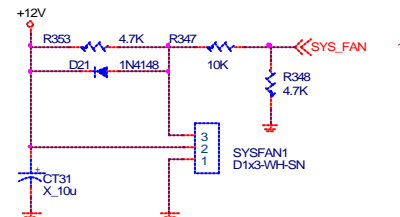


Add CPU FAN Speed control function

CPU FAN

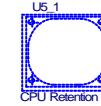
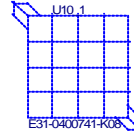
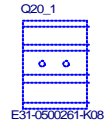
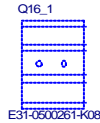
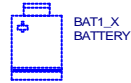
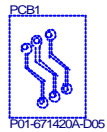


SYSTEM FAN

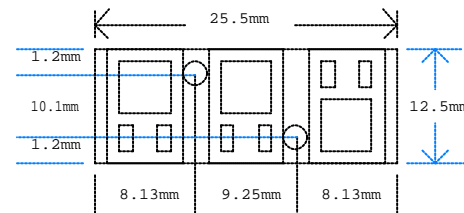
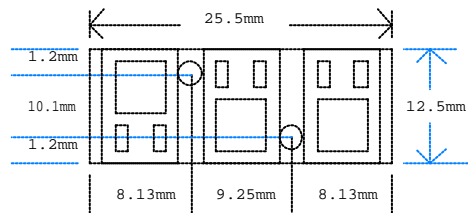
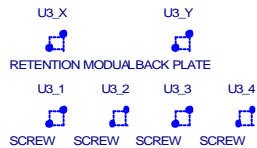
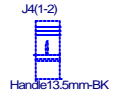


MICRO-STAR

Jumper Setting & Connector Setting



STD		
LAN		



		MICRO-STAR	
		JUMPER SETTING & MANUAL PARTS	
Size	Document Number	Rev	
	MS-6714	2.0A	
Date	Wednesday, February 26, 2003	Sheet	26 of 26

General SPEC

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	REQ#B (multifunction pin)
GPIO 2	I	Pull up through 8.2K ohms (PIRQE#)
GPIO 3	I	Pull up through 8.2K ohms (PIRQF#)
GPIO 4	I	Pull up through 8.2K ohms (PIRQG#)
GPIO 5	I	Pull up through 8.2K ohms (PIRQH#)
GPIO 6	I	Pull down through 10K ohms (unused)
GPIO 7	I	Pull down through 10K ohms (unused)
GPIO 8	I	Pull Up to 3.3VSBY through 4.7K ohms (SIO_PME)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifunction pin)
GPIO 12	I	EXTSMI# with Pull up 10K ohms to VCC3_SB
GPIO 13	I	Suspend mode selection jumper
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	GNT#B (multifunction pin)
GPIO 18*	O	No Connected
GPIO 19	O	No Connected
GPIO 20	O	No Connected
GPIO 21	O	No Connected
GPIO 22	OD	No Connected
GPIO 23	O	Pull Up to 3.3V through 8.2K ohms (BIOS protect)
GPIO 24	I/O	No Connected
GPIO 25	I/O	No Connected
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	No Connected
GPIO 28	I/O	No Connected
GPIO 29~31	O	Not Implemented
GPIO 32	I/O	No Connected
GPIO 33	I/O	No Connected
GPIO 34	I/O	Primary IDE ATA66/100 detection (PD_DET)
GPIO 35	I/O	Secondary IDE ATA66/100 detection (SD_DET)
GPIO 36	I/O	No Connected
GPIO 37	I/O	No Connected
GPIO 38	I/O	No Connected
GPIO 39	I/O	No Connected
GPIO 40	I/O	No Connected
GPIO 41	I/O	No Connected
GPIO 42	I/O	No Connected
GPIO 43	I/O	No Connected
GPIO 44~47	I/O	Not Implemented

* GPIO18 will toggle at 1Hz frequency.

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull down through 8.2K ohms (unused)
GPI 2	I	P1 customer defined
GPI 3	I	P1 customer defined
GPI 4	I	Pull down through 8.2K ohms (unused)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	REQ & GNT	CLOCK	CLK GEN PIN OUT	PCIRST#
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PREQ#0 PGNT#0	PCICLK0	10 (FS4/PCI3)	PCIRST#2
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PREQ#1 PGNT#1	PCICLK1	11 (PCI4)	PCIRST#2
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PREQ#2 PGNT#2	PCICLK2	12 (PCI5)	PCIRST#2
1394	INTF#	AD25	PREQ#4 PGNT#4	1394_PCLK	6 (FS2/PCI0)	PCIRST#1
LAN	INTG#	AD29	PREQ#3 PGNT#3	LAN_PCLK	15 (PCI7)	PCIRST#1

*PREQ#5 pull up to VCC3 through 8.2k Ohm

*ICH4 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.

DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0/DCLK0# DCLK1/DCLK1# DCLK2/DCLK2#
DIMM 2	1010001B	DCLK3/DCLK3# DCLK4/DCLK4# DCLK5/DCLK5#

Power Delivery Map

ATX P/S with 1A Stby current				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-10%

Processor
VCCVID
1.2V / 30mA
VCORE/Vtt
1.15V-1.75V
60A

Memory
Vdd/Vddq
2.5V / 5.92A
Vtt
1.25V / 2.1A

NB GMCH
VccCORE
1.5V / 2.46A
VccAGP
1.5V / 370mA
VccHI
1.5V / 90mA
VttFSB
1.15V-1.75V
2.4A
VccSM
2.5V / 2.8A
VccGPIO
3.3V / 30mA
Vcca_DAC
1.5V / 65mA
ICH4
VccCORE
1.5V / 970mA
VccHI
1.5V / 90mA
Vccsus1_5
1.5V / 85mA
V_CPU_IO
1.15V-1.75V
45mA
Vcc3_3
3.3V / 610mA
Vccsus3_3
3.3V / 70mA

CK-408
Vcc
3.3V / 280mA
LPC Super I/O
Vdd
3.3V / 25mA
FWH
Vdd
3.3V / 67mA

Net Name	Power	Device
+5VR	5V	Codec
+12V	12V	Serial port
+12VC	12V	SIO(HM)
+12VIN	12V	U18
-5V	-5V	SIO(HM)
-5VIN	-5V	SIO(HM)
-12V	-12V	Serial port
-12VC	-12V	SIO(HM)
-12VIN	-12V	SIO(HM)
9VSB	9V SB	
VCC1_5SB	1.5V SB	ICH4
VCC2_5	2.5V	D12
MEM_STR	2.5V	DDR
VCC3	3.3V	
VCC3_SB	3.3V SB	
VCC3_VID	3.3V	VID0~4
VCC5	5V	
VCC5_SB	5V SB	
VCC5_STR	5V Dual	USB
VCC_AGP	1.5V	
VCC_BUS	12V	1394
VCC_VID	1.2V	CPU
VCCA_DPLL	1.5V	GMCH
VCCA_FSB	1.5V	GMCH
VCCA_SM	1.5V	GMCH
VCCP	Vcore	
VCCQ_SM	2.5V	GMCH
VDD3	3.3V	Codec
VDD25	2.5V	LAN
VDD33	3.3V SB	LAN
VDDA3V	3.3V	CLK_Gen
VTIN_VCC	5V	SIO(HM)
VTT_DDR	1.25V	DDR

CNR Connector	
5V	1.0A
3.3V	1.0A
12V	0.5A
3.3Vaux	1.0A
-12V	0.1A
5VDual	0.5A

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

AGP Slot	
5V	2.0A
3.3V	6.0A
12V	1.0A
3.3Vaux	0.375A
1.5V	2.0A

USB
Vdd
5V / 2.0A

MICRO-STAR		
Title		
Power Delivery Map		
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	MS-6714	
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